AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of adding grant information to a memory ~~having a plurality of physical addresses where each physical address identifies an arbitration period~~ that stores information about a series of arbitration periods, the method comprising ~~the steps of~~:

~~if grant information is to be added to the memory, determining a number of desired arbitration periods requested by a communication circuit;~~

assigning a ~~range of logical addresses to the communication circuit, the number of logical addresses in the range being equal to the number of desired arbitration periods~~ number of first addresses to a group of devices such that two or more consecutive first addresses are assigned to each device and no two devices have the same first addresses, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, each first address having a sequence of bits; and

forming a number of ~~physical addresses by changing a number of the logical addresses in the range, each logical address having a corresponding physical address, a number of the physical addresses being spaced apart~~ second addresses from the number of the first addresses such that each first address has a corresponding second address and each second address has a corresponding device by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period.

2. (Currently Amended) The method of claim 1 and further comprising ~~the step of writing grant information for the communication circuit to the physical addresses that correspond with the logical addresses in the range~~ for each second address, writing grant information to the memory about the corresponding device.

3. (Currently Amended) The method of claim 2 wherein ~~the memory has a logical address that represents a next available arbitration period and the range of logical addresses are sequential~~ each device is assigned only consecutive first addresses.

4. (Currently Amended) The method of claim 3 wherein ~~a value that represents the logical address of the next available arbitration period is updated by adding the number of logical addresses in the range to a prior value that represented the logical address of the next available arbitration period when a range is defined~~ first addresses are assigned to a first device, and second addresses are formed for the first device before first addresses are assigned to a second device.

Claims 5-6 (Cancelled)

7. (Currently Amended) The method of claim [[6]] 1 wherein ~~the~~ forming ~~step~~ further includes ~~the steps of~~:

setting a least significant bit of a ~~physical~~ second address to have a value equal to a most significant bit in a ~~logical~~ first address; and

setting a first next to the least significant bit of the ~~physical~~ second address to have a value equal to a first next to the most significant bit in the ~~logical~~ first address.

8. (Currently Amended) The method of claim 7 and further comprising ~~the step of~~ setting a second next to the least significant bit of the ~~physical~~ second address to have a value equal to a second next to the most significant bit in the ~~logical~~ first address.

9. (Cancelled)

10. (Currently Amended) The method of claim [[6]] 1 wherein ~~the~~ forming ~~step~~ further includes ~~the steps of~~:

gray encoding a ~~logical~~ first address to form an intermediate address;

setting a least significant bit of a ~~physical~~ second address to have a value equal to a most significant bit in the intermediate address; and

setting a first next to the least significant bit of the ~~physical~~ second address to have a value equal to a first next to the most significant bit in the intermediate address.

11. (Cancelled)

12. (Currently Amended) The method of claim ~~11~~ 10 and further comprising ~~the step of~~ setting a second next to the least significant bit of the ~~physical~~ second address to have a value equal to a second next to the most significant bit in the ~~logical~~ intermediate address.

Claims 13-15 (Cancelled)

16. (Currently Amended) A communications circuit comprising:

a transmit circuit that transmits information onto a bus;

a receive circuit that receives information from the bus;

a memory that ~~has a plurality of physical addresses where each physical address identifies an arbitration period~~ stores information on a series of arbitration periods; and

a logic circuit connected to the transmit circuit, the receive circuit, and the memory, if grant information for a group of devices is to be added to the memory, the logic circuit ~~determines a number of desired arbitration periods requested by a communication circuit, and assigns a range of logical addresses that identify the communication circuit, the number of logical addresses in the range being equal to the number of desired arbitration periods~~ assigns a number of first addresses to the group of devices such that two or more consecutive first addresses are assigned to each device and no two devices have the same first addresses, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, each first address having a sequence of bits.

17. (Currently Amended) The communications circuit of claim 16 wherein the logic circuit forms a number of ~~physical addresses by changing a number of the logical addresses in the range, each logical address having a corresponding physical address, a number of the physical addresses being spaced apart~~ second addresses from the number of the first addresses such that each first address has a corresponding second address and each second address has a corresponding device by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period.

18. (Currently Amended) The communications circuit of claim 17 wherein the logic circuit forms the ~~physical~~ second addresses by:

setting a least significant bit of a ~~physical~~ second address to have a value equal to the most significant bit in a ~~logical~~ first address; and

setting a first next to the least significant bit of the ~~physical~~ second address to have a value equal to a first next to the most significant bit in the ~~logical~~ first address.

19. (Currently Amended) The communications circuit of claim 17 wherein the logic circuit forms the ~~physical~~ second addresses by:

gray encoding a ~~logical~~ first address to form an intermediate address;

setting a least significant bit of a ~~physical~~ second address to have a value equal to the most significant bit in the intermediate address; and

setting a first next to the least significant bit of the ~~physical~~ second address to have a value equal to a first next to the most significant bit in the intermediate address.

20. (Cancelled)

21. (New) A method of adding grant information to a memory that stores information about a series of arbitration periods, the method comprising:

assigning a number of first addresses to a device, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, each first address having a sequence of bits; and

forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address by rearranging the sequence of bits in a plurality of the number of first addresses, the first addresses and second addresses having an equal number of bits, each second address representing one arbitration period.

22. (New) The method of claim 21 and further comprising storing information in the memory about the device at each location defined by a second address.

23. (New) The method of claim 22 wherein the rearranging includes:

setting a least significant bit of a second address to have a value equal to a most significant bit in a first address; and

setting a first next to the least significant bit of the second address to have a value equal to a first next to the most significant bit in the first address.

24. (New) The method of claim 23 wherein the rearranging further includes setting a second next to the least significant bit of the second address to have a value equal to a second next to the most significant bit in the first address.

25. (New) The method of claim 22 wherein forming further includes:

gray encoding a first address to form an intermediate address;

setting a least significant bit of a second address to have a value equal to a most significant bit in the intermediate address; and

setting a first next to the least significant bit of the second address to have a value equal to a first next to the most significant bit in the intermediate address.

26. (New) A method of adding grant information to a memory that stores information on a series of arbitration periods, the method comprising:

assigning a number of first addresses to a device, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period, no two first addresses being identical, each first address having a sequence of bits; and

forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period, no two second addresses being identical.

27. (New) The method of claim 26 and further comprising storing information in the memory about the device at each location defined by a second address.

28. (New) The method of claim 27 wherein the rearranging includes:

setting a least significant bit of a second address to have a value equal to a most significant bit in a first address; and

setting a first next to the least significant bit of the second address to have a value equal to a first next to the most significant bit in the first address.

29. (New) The method of claim 28 wherein the rearranging further includes setting a second next to the least significant bit of the second address to have a value equal to a second next to the most significant bit in the first address.

30. (New) The method of claim 26 wherein forming further includes:

gray encoding a first address to form an intermediate address;

setting a least significant bit of a second address to have a value equal to a most significant bit in the intermediate address; and

setting a first next to the least significant bit of the second address to have a value equal to a first next to the most significant bit in the intermediate address.